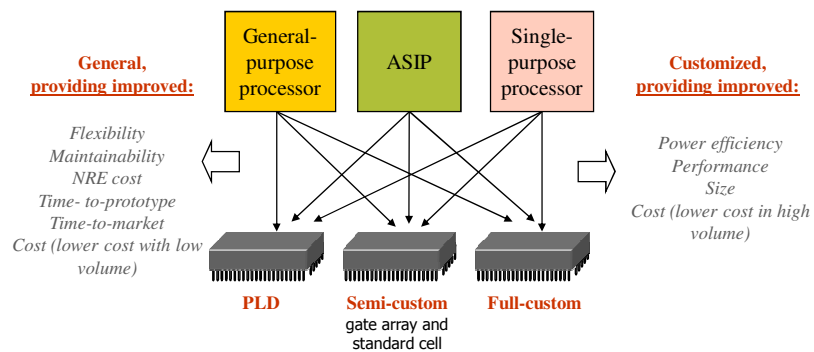


Research in Hardware/Software Co-design

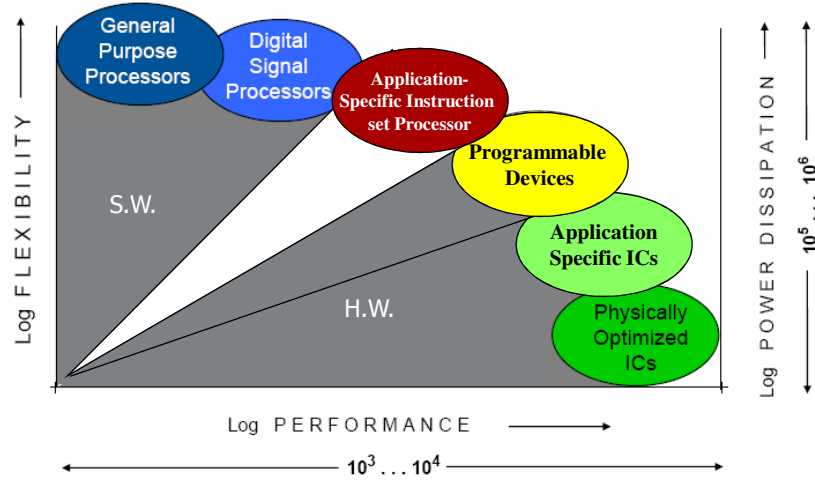
Dr. Issam Damaj
Assistant Professor of
Electrical and Computer Engineering

Independence of Processor and IC technologies

- Basic tradeoff
 - General vs. custom
 - With respect to processor technology or IC technology
 - The two technologies are independent



The Boarder

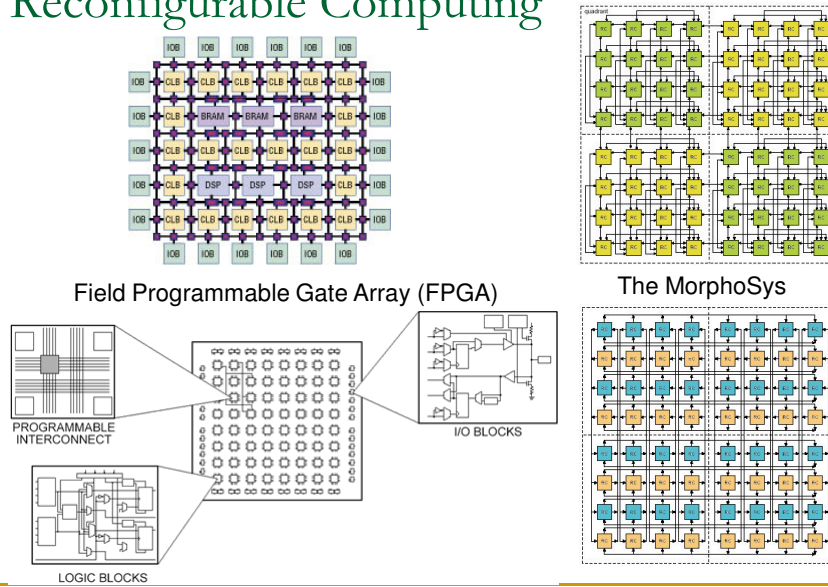


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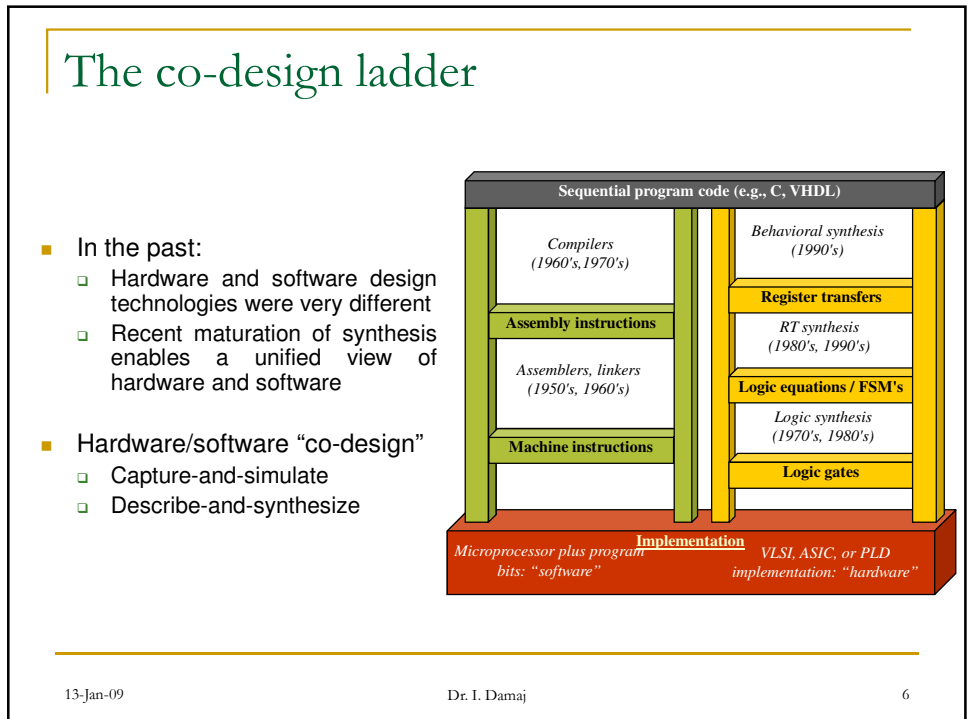
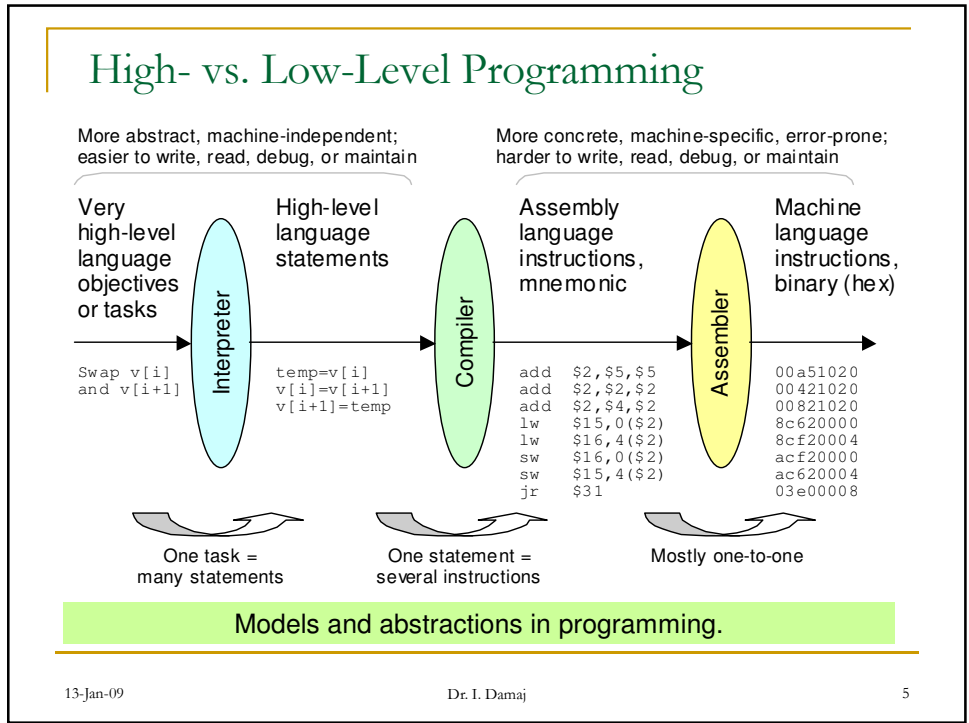
Reconfigurable Computing



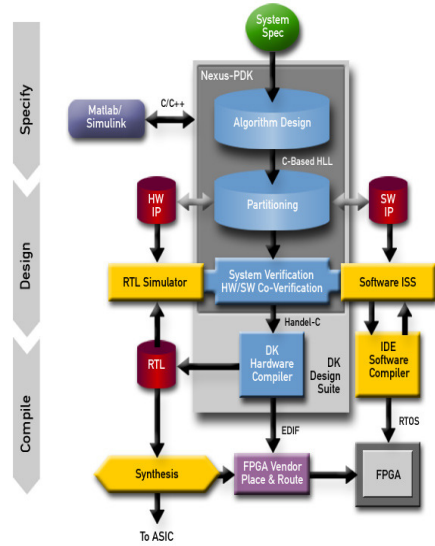
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Compiled System Design Flow - Agility U.K.

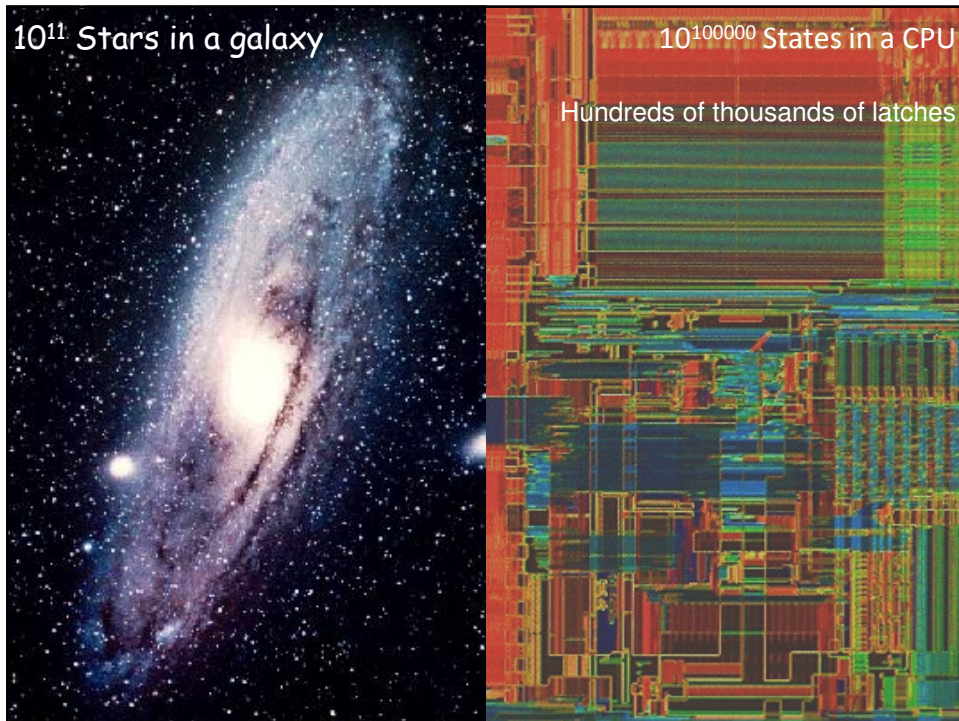


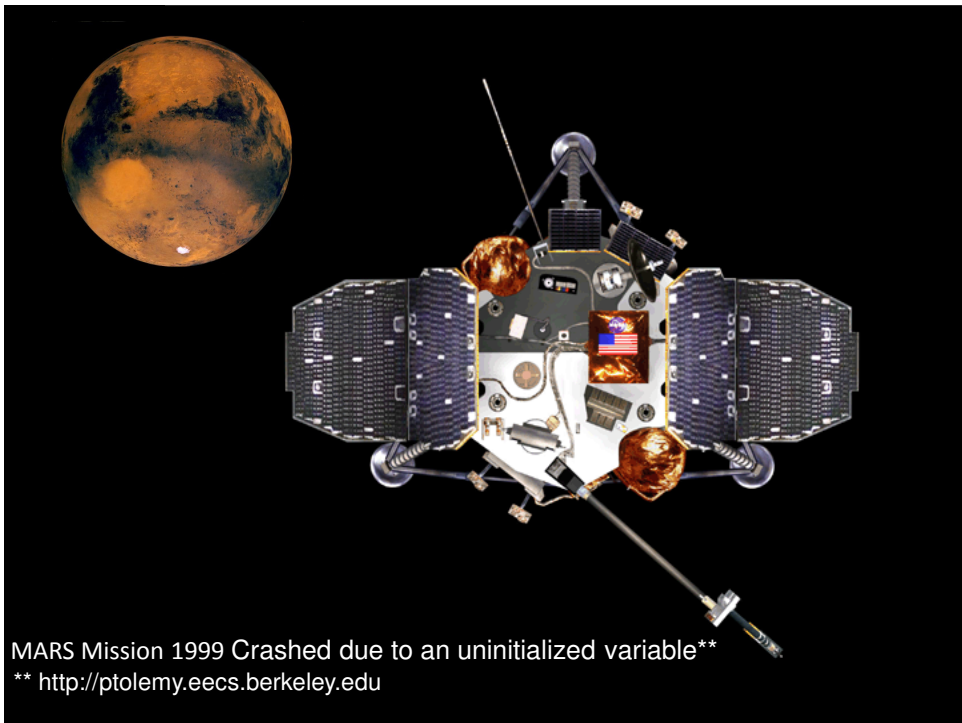
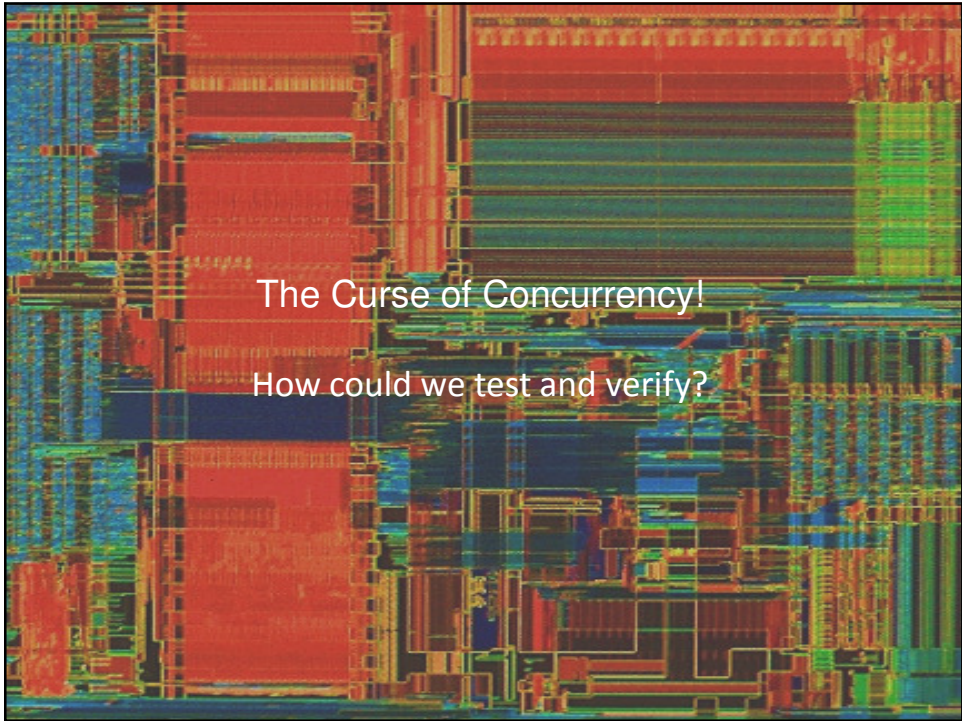
- Hardware/Software Co-design
- Hardware/Software Co-verification
- Hardware/Software Interface Design
- High-level Hardware Development

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Could we go even to higher levels of abstraction in design?

Could we reach the highest possible degree of parallelism?

How fast could we go?

To what minimum the logic area of a design could be reduced?

How much power could we save?

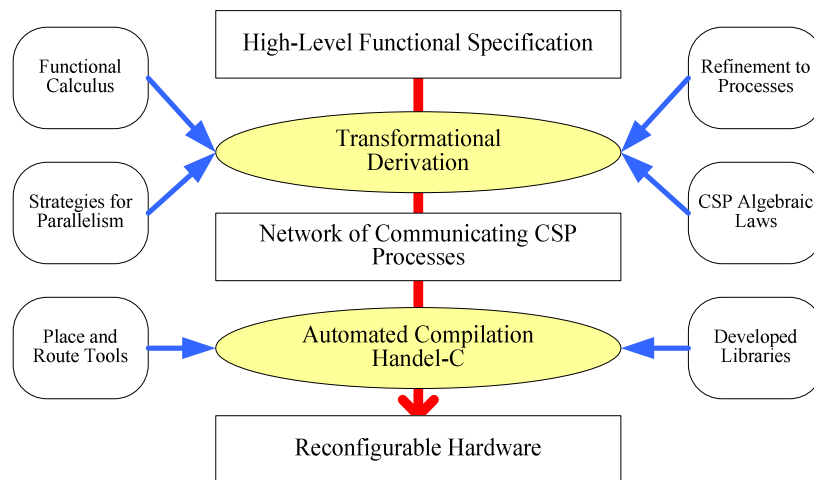
What about correctness, testing and verification?

Who could deal with such a hybridization of disciplines?

High-level Hardware Development

Maybe Higher-level?

Synthesis of Massively Parallel Algorithms and their Mapping onto Reconfigurable Hardware



Functional Programming

- Functions are considered as the basic unit of program development and as the major routes to reuse.
- Few fundamental advantages of using FP is
 - High-level of abstraction through its powerful set of high-order functions.
 - Clarity.
 - Conciseness
 - Correctness that could be proved or insured by construction.
- The attractions for using the functional paradigm in hardware development incited many researchers, such as, *Lava*, *Hawk*, *Hydra*, *HML*, *MHDL*, *DDD* system, *SAFL*, *MuFP*, *Ruby*, and *Form*.

$$\text{zipWith} :: [A] \rightarrow [B] \rightarrow [C]$$

$$\text{zipWith } (\oplus) [x_1, x_2, \dots, x_n] [y_1, y_2, \dots, y_n] = [x_1 \oplus y_1, x_2 \oplus y_2, \dots, x_n \oplus y_n]$$

$$\text{foldr}(\oplus)[x_1 \ x_2 \ \dots \ x_n] = x_1 \oplus x_2 \oplus \dots \oplus x_n$$

$$\text{vscalarp} :: [Int] \rightarrow [Int] \rightarrow Int$$

$$\text{vscalarp } \text{as } \text{bs} = \text{foldr}(+) (\text{zipWith}(\ast) \text{as } \text{bs})$$

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Communicating Sequential Processes (CSP)

- CSP notation is based on events and processes.
- A CSP process engages in a series of events, which can be channel-based communication with synchronization capabilities.
- Major work in hardware design:
 - The compiled *Occam* into *FPGAs*
 - *Handel-C* compiler
 - Translation between CSP and *Handel-C*.

$$\text{ADD} = (\text{in}_1 ? a \rightarrow \text{SKIP} \parallel \text{in}_2 ? b \rightarrow \text{SKIP}); \text{out} ! a + b \rightarrow \text{SKIP}$$

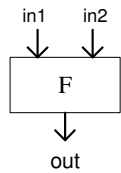
$$\text{MUL} = (\text{in}_1 ? a \rightarrow \text{SKIP} \parallel \text{in}_2 ? b \rightarrow \text{SKIP}); \text{out} ! a * b \rightarrow \text{SKIP}$$

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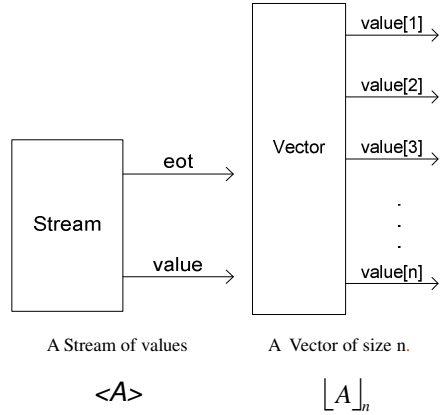
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Refinement



The Process F refinement of a function f

Process Refinement



Data Refinement

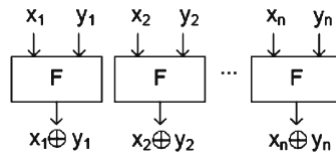
Refinement of High-order Functions

$$zipWith :: [A] \rightarrow [B] \rightarrow [C]$$

$$zipWith (\oplus) [x_1, x_2, \dots, x_n] [y_1, y_2, \dots, y_n] = [x_1 \oplus y_1, x_2 \oplus y_2, \dots, x_n \oplus y_n]$$

$$vzip (\oplus) :: [A]_n \rightarrow [B]_n \rightarrow [C]_n$$

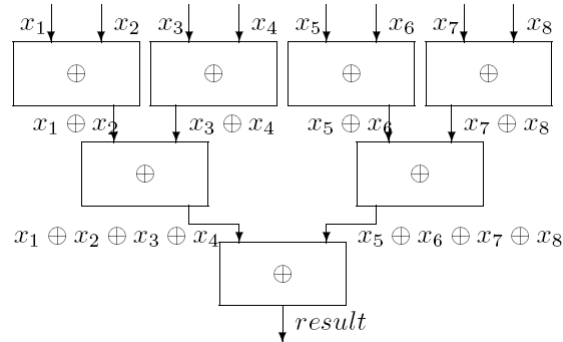
$$VZIP =_{i=1}^n F[out_i/out, c_i/in_1, d_i/in_2]$$



Refinement of High-order Functions

$$\text{foldr}(\oplus)[x_1 \ x_2 \ \dots \ x_n] = x_1 \oplus x_2 \oplus \dots \oplus x_n$$

$$\text{VFOLD}_n(F) = \prod_{i=1}^n F[c_i/\text{out}, c_{2i}/\text{in}_1, c_{2i+1}/\text{in}_2]$$



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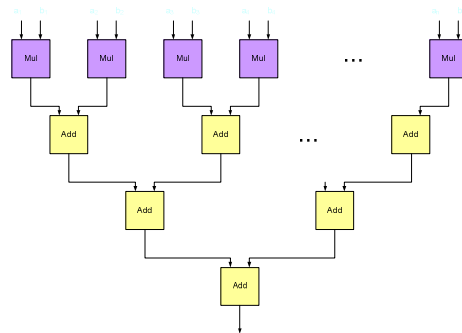
Scalar Product

$$\text{vscalarp} :: [\text{Int}] \rightarrow [\text{Int}] \rightarrow \text{Int}$$

$$\text{vscalarp } \text{as } \text{bs} = \text{foldr}(+) (\text{zipWith}(\ast) \text{ as } \text{bs})$$

$$\text{vscalarp} :: [\text{Int}]_m \rightarrow [\text{Int}]_m \rightarrow \text{Int}$$

$$\text{VSCALARP} = \text{VZIP}_m(\text{MUL}) \gg_m \text{VFOLD}_m(\text{ADD})$$



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Handel-C

```

macro proc VScalarP (As, Bs, Size, OutputItem)
{
  par
  {
    VZipWith (Size, As, Bs, InternalV, Multiplication);
    VFoldR (InternalV, OutputItem, Size, Addition, 0);
  }
}

```

Simple Example: Rijndael Single Round

```

singleRound :: State -> State -> State
singleRound stateIn sKeys =
  addRoundKey ((mixColumns shiftRows subBytes) stateIn) sKeys

singleRound :: [Int8]_4 -> [Int8]_4 -> [Int8]_4
singleRound 0 SINGLEROUND
SINGLEROUND = (SUBBYTES >> SHIFTRows >> MIXCOLUMNS) || ADDROUNDKEY

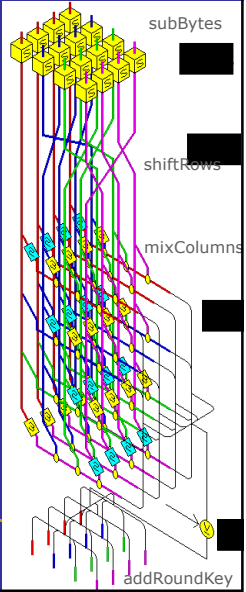
macro proc SingleRound
  (vovStateIn, vovKStateIn, vovStateOut) {
  par{
    SubBytes (vovStateIn, sosOut1);
    ShiftRows (sosOut1, sovOut2);
    MixColumns (sovOut2, vovOut3);
    AddRoundKey (vovOut3, vovKStateIn, vovStateOut);}}

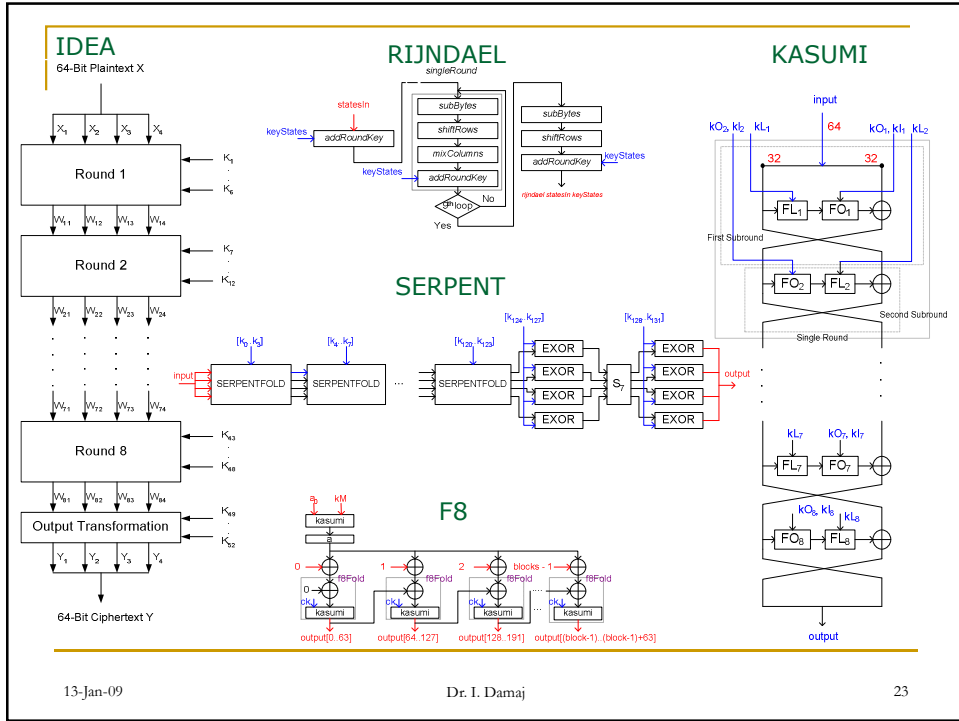
```

Functional Specification

CSP

Handel-C

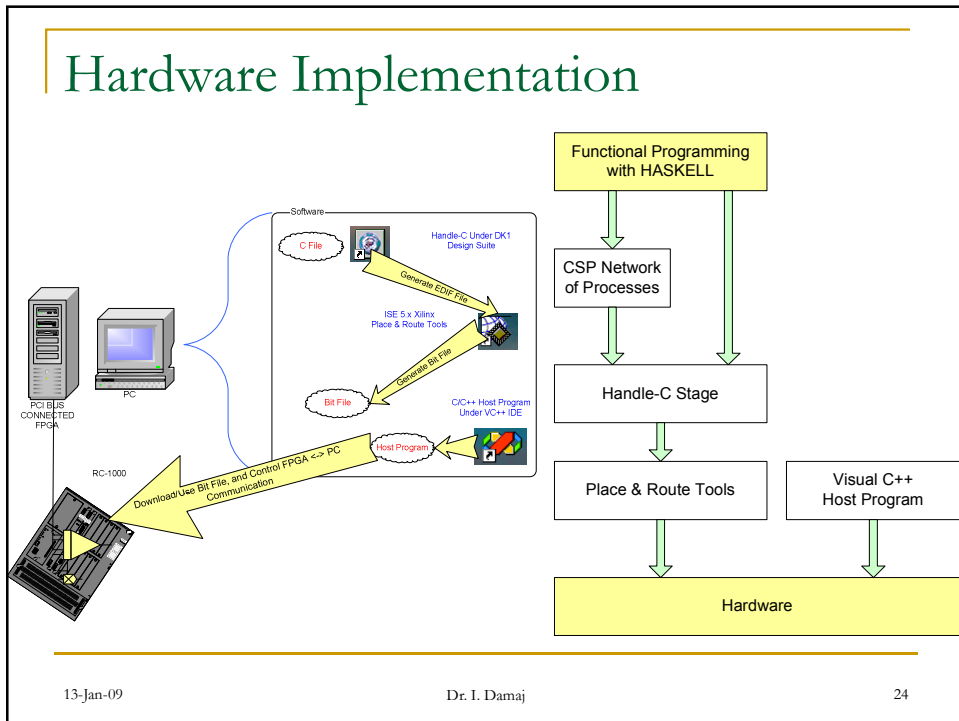




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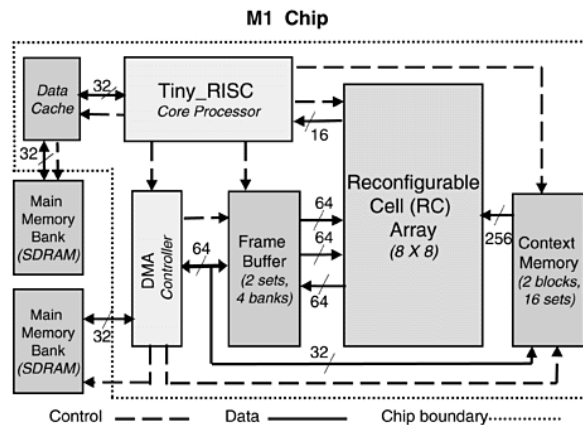
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Performance Evaluation of Dynamic Reconfigurable Systems

The MorphoSys

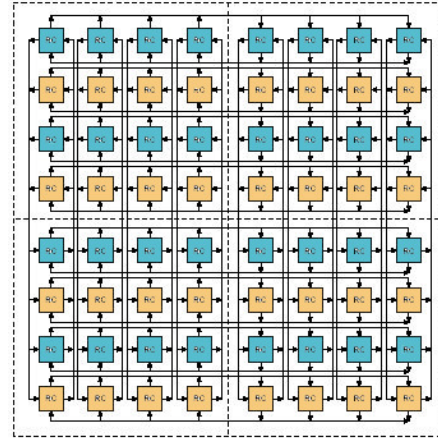
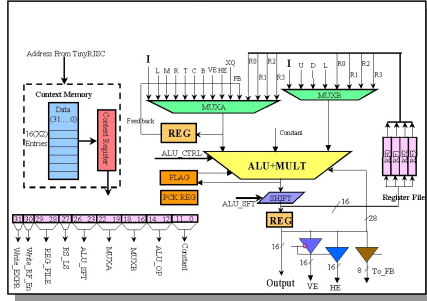
The MorphoSys

- Computer Graphics
- Information Coding
- Cryptography
- Networking



The MorphoSys

UCI Re-configurable Cell MorphoSys



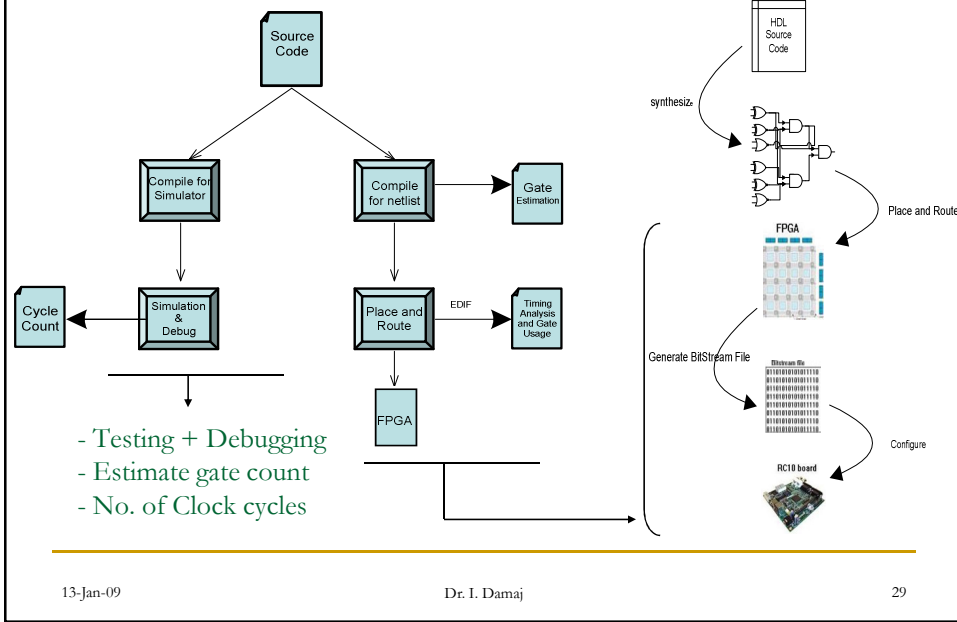
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High-speed Hardware Cores

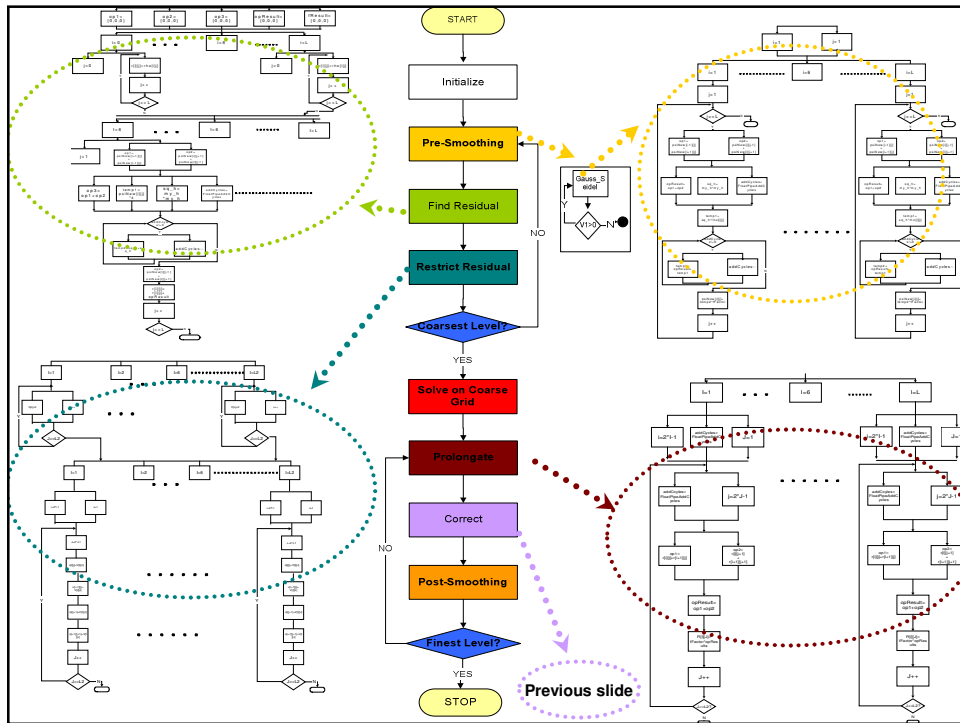
Iterative Solvers: Multigrid, Jacobi, and SOR

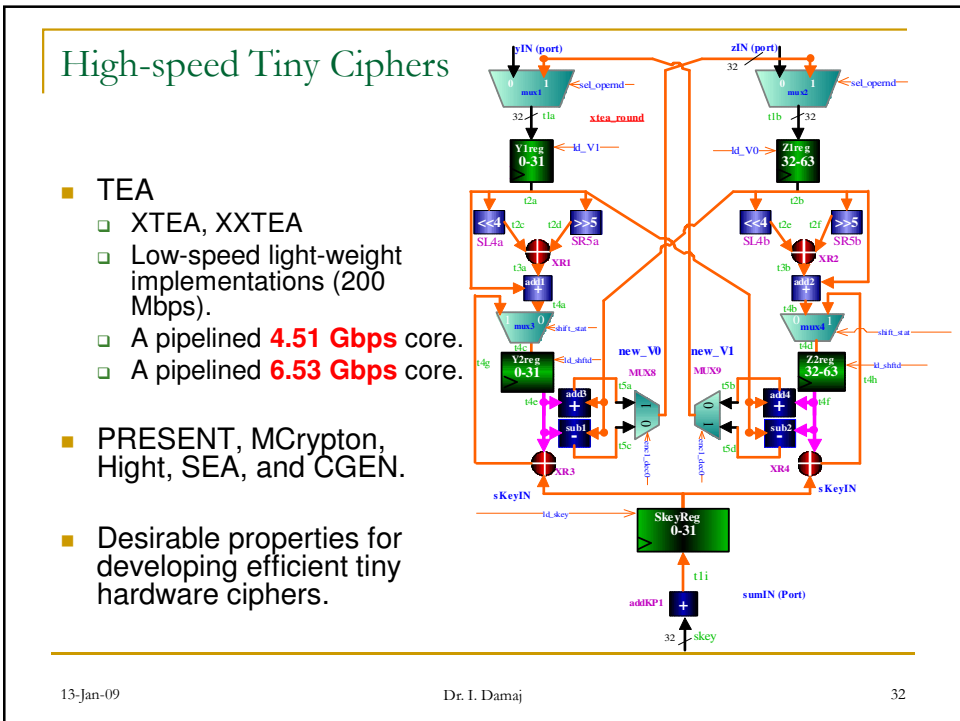
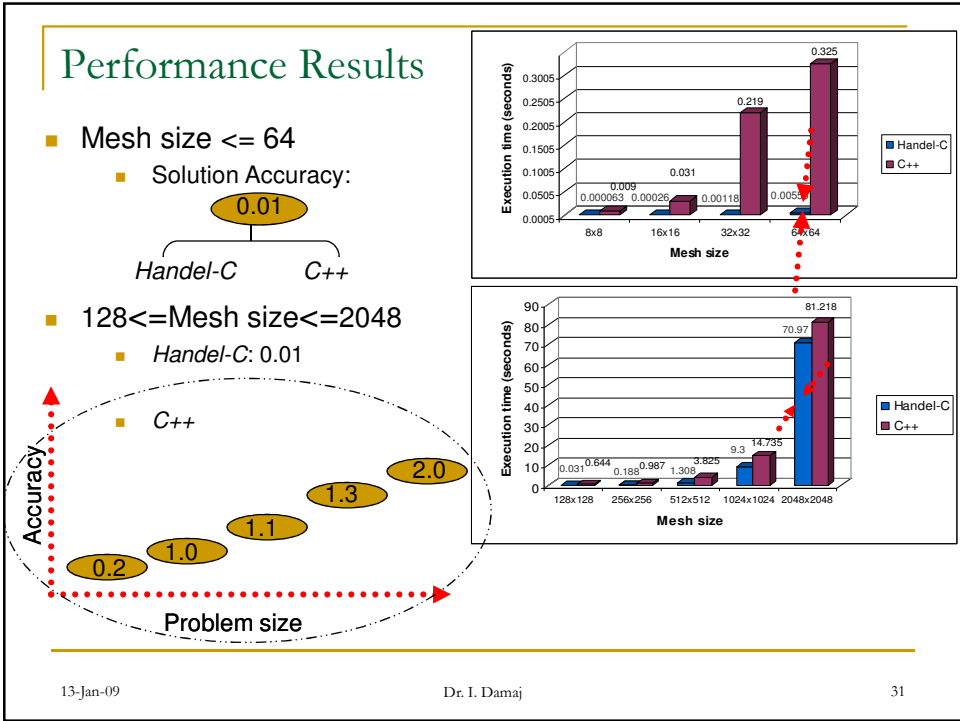


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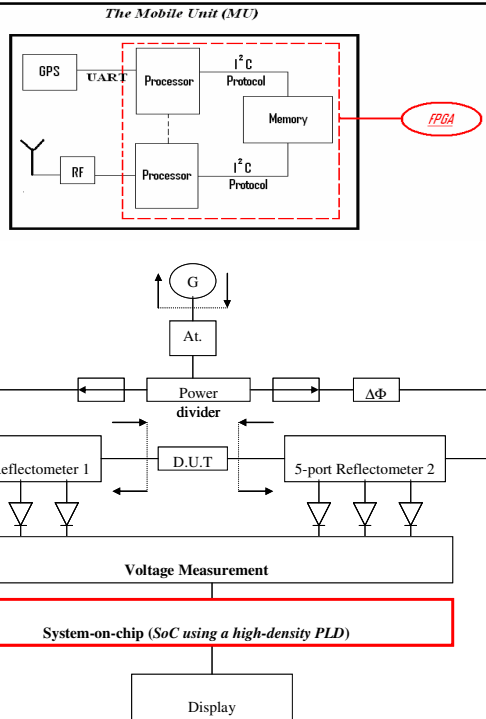
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FPGAs

- Promoting FPGAs as a suitable replacement for traditional microcontrollers in specific applications.
- The Aram Locator GPS-based Vehicle Tracking System
- An Embedded Nine-Port Microwave Vector Network Analyzer



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<http://academics.idamaj.net/>

Questions?

Thank You